

FORM PCT 1390
REV. 5/93

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NO
SCHAUER ET AL -1 (PCT)

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO (if known, see 37 CFR 1.5)

09/890656

INTERNATIONAL APPLICATION NO.
PCT/EP00/01800

INTERNATIONAL FILING DATE
MARCH 2, 2000

PRIORITY DATE CLAIMED
MARCH 4, 1999

TITLE OF INVENTION

SEMICONDUCTOR WAFER COMPRISING A THIN EPITAXIAL SILICON LAYER AND METHOD FOR
PRODUCING SAME

APPLICANT(S) FOR DO/EO/US

REINHARD SCHAUER; MARKUS BLIETZ; WILFRIED von AMMON; RÜDIGER SCHMOLKE

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371 (f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(l).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau)
 - b. ☐ has been transmitted by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
 - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☐ have been transmitted by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
 - d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

Applicant Claims Priority under 35 U.S.C. §119 of German Application No. No. 199 09 557.4 filed March 4, 1999.
Applicant Claims Priority under 35 U.S.C. §119 of German Application No. No. 100 04 623.1 filed February 3, 2000
Applicant Claims Priority under 35 U.S.C. §120 of: PCT No. PCT/EP00/01800 filed March 2, 2000

APPLICATION NO. (if known, see 37 CFR 1.5)

09/890656

INTERNATIONAL APPLICATION NO
PCT/EP00/10800ATTORNEY'S DOCKET NO
SCHAUER ET AL
(PCT)☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO.....\$860.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)

.....\$690.00

Neither international preliminary examination fee paid (37 CFR 1.82) nor
international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....\$1,000.00International preliminary examination fee paid to USPTO (37 CFR 1.482)
and all claims satisfied provisions of PCT Article 33(2)-(4).....\$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =

\$ 860.00

PTO USE ONLY

Surcharge of \$130.00 for furnishing the oath or declaration later than ____ 20 ____ 30
months from the earliest claimed priority date (37 CFR 1.492(e)).

Claims	Number Filed	Number Extra	Rate		
Total Claims	12 - 20 =	- 0 -	X \$18.00	\$	
Independent Claims	3 - 3 =	- 0 -	X \$80.00	\$	
Multiple dependent claim(s) (if applicable)			+ \$270.00	\$	
TOTAL OF ABOVE CALCULATIONS =				\$	
Reduction by 1/2 for Small Entity status.				\$	
SUBTOTAL =				\$ 860.00	
Processing fee of \$130.00 for furnishing the English translation later than ____ 20 ____ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	
TOTAL NATIONAL FEE =				\$ 860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				See cover sheet attached to assign \$ to be charged to Deposit Acct	
TOTAL FEES ENCLOSED =				\$ 860.00	
				Amount to be: refunded	\$
				charged	\$

☐ Applicant claims Small Entity status.a. ☒ A check in the amount of \$ 860.00 to cover the above fees is enclosed.b. ☐ Please charge my Deposit Account No. 03-2468 in the amount of \$ to cover the above fees. A duplicate
copy of this sheet is enclosed.c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any
overpayment, to Deposit Account No. 03-2468. A duplicate copy of this sheet is enclosed.**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or
(b)) must be filed and granted to restore the application to pending status.**


SEND ALL CORRESPONDENCE TO:

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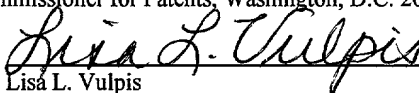
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Edward R. Freedman

Reg. No. 26,048

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Date of Deposit AUGUST 2, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37
CFR 1.10, on the date indicated above, and is addressed to the Ass't. Commissioner for Patents, Washington, D.C. 20231


Lisa L. Vulpis

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: SCHAUER ET AL 1 PCT

PCT SERIAL No: PCT/EP00/01800

PCT FILED: MARCH 2, 2000

PRIORITY: 199 09 557.4

PRIORITY FILED: MARCH 4, 1999

PRIORITY: 100 04 623.1

PRIORITY FILED: FEBRUARY 3, 2000

TITLE: SEMICONDUCTOR WAFER COMPRISING A THIN EPITAXIAL
SILICON LAYER AND METHOD FOR PRODUCING THE SAME

PRELIMINARY AMENDMENT

ATT: BOX PCT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Preliminary to examination please amend the above-identified
U.S. National Phase U.S. patent application as follows:

IN THE ABSTRACT:

Please insert the enclosed Abstract of the Disclosure attached
hereto on its own separate page.

IN THE SPECIFICATION:

Please amend the Specification as follows:

On page 1, above the first paragraph and below the title,
please insert the following paragraphs:

09/890656-00000000

--CROSS REFERENCE TO RELATED APPLICATIONS

Applicants claim priority under 35 U.S.C. §119 of German Patent Application Serial No. 199 09 557.4, filed on March 4, 1999 and German Patent Application Serial No. 100 04 623.1 filed February 3, 2000. Applicants also claim priority under 35 U.S.C. §120 of International Application PCT/EP00/01800, filed on March 2, 2000. The International Application under PCT article 21(2) was not published in English.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a semiconductor wafer with a thin epitaxial layer, and a process for producing the semiconductor wafer by depositing the layer on a substrate wafer made of monocrystalline silicon.--

On page 1 between the first paragraph and the second paragraph, please insert the following paragraphs:

-- 2. The Prior Art

EP-829559 A1 discloses a process for producing semiconductor wafers with a low defect density, it being necessary to provide a single crystal which has to be pulled with forced cooling or has to have a specific oxygen and nitrogen

concentration, and semiconductor wafers obtained from the single crystal having to be subjected to heat treatment. EP-644588 A1 relates to a semiconductor wafer having an epitaxially provided layer which has a low defect density and originates from a single crystal pulled at a pulling rate of at more 0.6 mm/min.--

On page 2, between the top paragraph and the first complete paragraph on this page, please insert:

--SUMMARY OF THE INVENTION--

On Page 2, please cancel the second complete paragraph on this page, and please rewrite by replacing with the following paragraph:

--The invention relates to a semiconductor wafer comprising a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon, which is characterized in that the substrate wafer has a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$, and a nitrogen concentration of from 1×10^{-13} to $5 \times 10^{15} \text{ atcm}^{-3}$, and the epitaxial layer has a thickness of from 0.2 to 1.0 μm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.--

On page 6, in the line above the word "Example", please insert:

-- DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS--

A Marked-up Version of Amended Specification Pages 1, 2 and 6 is enclosed.

IN THE CLAIMS:

Please cancel claims 1 to 12 without prejudice, and please insert new claims 13 to 24.

13. A semiconductor wafer, comprising
a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon;
said substrate wafer having a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from 1×10^{13} to $5 \times 10^{15} \text{ atcm}^{-3}$; and
the epitaxial layer has a thickness of from 0.2 to 1.0 μm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.

14. The semiconductor wafer as claimed in claim 13,
wherein the oxygen concentration of the substrate wafer is less than $6.5 \times 10^{17} \text{ atcm}^{-3}$.

15. The semiconductor wafer as claimed in claim 13,
wherein the nitrogen concentration of the substrate wafer lies in a range of from 1×10^{14} to $5 \times 10^{14} \text{ atcm}^{-3}$.

16. A process for producing a semiconductor wafer with an epitaxial layer by depositing the layer on a substrate wafer made of monocrystalline silicon, by a sequence of steps comprising:

providing a substrate wafer, having a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from 1×10^{13} to $5 \times 10^{15} \text{ atcm}^{-3}$;

heating the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C to 1170°C ; and

immediately after the deposition temperature has been reached, depositing of the epitaxial layer with a thickness of from 0.2 to 1.0 μm .

17. A process for producing a semiconductor wafer with an epitaxial layer by depositing the layer on a substrate wafer made of monocrystalline silicon, by a sequence of steps comprising:

providing a substrate wafer by separating the substrate wafer from a single crystal which has been pulled according to the Czochralski process and subjected to forced cooling,

said substrate wafer having a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ to $5 \times 10^{15} \text{ atcm}^{-3}$;

heating of the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C ; and

immediately after the deposition temperature has been reached, depositing the epitaxial layer with a thickness of from 0.2 to 1.0 μm .

18. The process as claimed in claim 16, comprising
pulling a single crystal from a melt in accordance with
the Czochralski process, and at least 90 minutes elapsing before
the single crystal has passed through a temperature range of from
1050°C to 900°C, the single crystal serving as a source for the
providing of the substrate wafer, and the deposition temperature
during the depositing of the epitaxial layer is from 1120°C to
1170°C.

19. The process as claimed in claim 16, comprising
pulling a single crystal from a melt in accordance with
the Czochralski process and not more than 40 minutes elapsing
before the single crystal, with application of forced cooling, has
passed through the temperature range from 1050°C to 900°C, the
single crystal serving as a source for the providing of the
substrate wafer, and the deposition temperature during the
depositing of the epitaxial layer is from 1120°C to 1200°C.

20. The process as claimed in claim 19,
wherein the deposition temperature is from 1130°C to
1190°C.

21. The process as claimed in claim 16, comprising
heating the substrate wafer to the deposition temperature
in a gas atmosphere being selected from the group of gases
consisting of hydrogen, argon, helium and mixtures of these gases.

22. The process as claimed in claim 16, comprising
depositing the epitaxial layer in a deposition atmosphere
containing a deposition gas and a dopant gas, the deposition gas
being selected from the group of gases consisting of
trichlorosilane, silane, dichlorosilane, tetrachlorosilane and
mixtures of these gases; and the dopant gas is selected from the
group of gases consisting of diborane, phosphine and arsine.

23. The process as claimed in claim 16, comprising
depositing the epitaxial layer within a deposition time
of from 1 to 10 s.

24. The process as claimed in claim 16, comprising
cleaning the deposition reactor with an etching gas or
plasma at the earliest after an epitaxial layer has been deposited
on 50 substrate wafers in succession.

REMARKS

The amendments to this patent application are as follows. An
Abstract of the Disclosure on its own separate sheet has been
added. The Specification has been amended to include a cross
reference to related applications and to include changes made in
the International Office. The specification has also been amended
to include the section headings required by U.S. practice.
Amendments to the claims are to remove the multiple dependency of

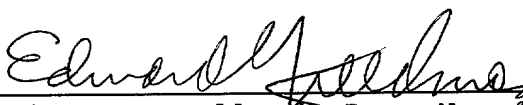
certain claims, and to include revisions made in the International Office.

No new matter has been introduced by this Amendment. Entry and consideration of this Amendment is respectfully requested.

Respectfully submitted,

Reinhard SCHAUER ET AL 1 PCT

By:


Allison C. Collard, Reg. No. 22,532
Edward R. Freedman, Reg. No. 26,048
Attorneys for Applicant

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Encl.: 1. Abstract of the Disclosure
2. Marked-up Version of Pages 1, 2 and 6 of the Specification

Express Mail No. EL 871 446 549 US

Date of Deposit AUGUST 2, 2001

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Lisa L. Vulpis

ABSTRACT OF THE DISCLOSURE

A semiconductor wafer is made of a silicon substrate wafer and an epitaxial silicon layer deposited thereon. The substrate wafer has a specific resistance of 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of 1×10^{13} to $5 \times 10^{15} \text{ atcm}^{-3}$. The epitaxial layer is 0.2 to 1.0 μm thick and has a surface on which fewer than 30 LLS (localized light scattering) defects which are greater in size than 0.085 μm can be detected. A method for producing the semiconductor wafer has a sequence of steps for providing the substrate wafer with the aforementioned features; heating the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C; and depositing the epitaxial layer thereon with a thickness of 0.2 to 1.0 μm , immediately after the deposition temperature has been reached.

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JC05 Rec'd PCT/PTO 0 2 AUG 2001

MARKED-UP VERSION

OF SPECIFICATION

09/890656-000201

09/890656

JCS Rec'd PCT/PTO

02 AUG 2001

Semiconductor wafer with a thin epitaxial layer, and

process for producing the semiconductor wafer

CROSS-REFERENCE TO RELATED APPLICATIONS

1. Field OF THE INVENTION

The invention relates to a semiconductor wafer with a
5 thin epitaxial layer, and a process for producing the
semiconductor wafer by depositing the layer on a
substrate wafer made of monocrystalline silicon.

2. The Prior Art

EP-829559 A1 discloses a process for producing
10 semiconductor wafers with a low defect density, it
being necessary to provide a single crystal which has
to be pulled with forced cooling or has to have a
specific oxygen and nitrogen concentration, and
semiconductor wafers obtained from the single crystal
15 having to be subjected to heat treatment. EP-644588 A1
relates to a semiconductor wafer having an epitaxially
provided layer which has a low defect density and
originates from a single crystal pulled at a pulling
rate of at most 0.6 mm/min.

At the present time intensive investigations are under
way with the aim of establishing which features
semiconductor wafers with an epitaxial layer have to
have in order to qualify them as a base material for
25 the production of modern CMOS components. According to
the publication in Jpn. J. Appl. Phys. Vol. 36 (1997),
pp. 2565-2570, a semiconductor wafer comprising a
p⁻-doped substrate wafer and a likewise p⁻-doped
epitaxial layer having a thickness of 1 μ m is
30 particularly suitable for large scale integrated CMOS
applications. This appraisal is also supported by the
publication in Electrochemical Society Proceedings
Volume 98-1, pp. 855-861. However, this paper also
draws attention to light-scattering defects (light
35 point defects) on the surface which occur in a
semiconductor wafer with a thin epitaxial layer but do
not adversely affect the GOI (gate oxide integrity).

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The abovementioned defects are called LLSs (localized light scatterers) by experts. Despite their indifferent behavior with regard to the GOI, the LLSs are undesirable to manufacturers of integrated circuits, which is also demonstrated by the fact that the ITRS (International Roadmap For Semiconductors) demands that the number of LLSs with a size of greater than or equal to $0.085\text{ }\mu\text{m}$ be less than or equal to 38 per semiconductor wafer with an epitaxial layer. This requirement applies to $0.18\text{ }\mu\text{m}$ technology and it must be assumed that as miniaturization advances ($0.13\text{ }\mu\text{m}$ and below), an even more stringent requirement will be imposed on the number of LLSs. Moreover, the limit value of 38 LLSs represents a maximum value and it should be taken into account that the number required for an industrial process capability must be significantly less than that.

SUMMARY OF THE INVENTION

The object of the invention was to provide a semiconductor wafer with an epitaxial layer which is suitable for modern CMOS applications, has a particularly small number of LLSs and requires comparatively low production costs. The object of the invention is, moreover, to specify a process for producing the semiconductor wafer.

The invention relates to a semiconductor wafer, comprising a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon, which is characterized in that the substrate wafer has a resistivity of from 0.1 to $50\text{ }\Omega\text{cm}$, an oxygen concentration of less than $7.5 \cdot 10^{17}\text{ atcm}^{-3}$ and a nitrogen concentration of from $1 \cdot 10^{13}$ to $5 \cdot 10^{15}\text{ atcm}^{-3}$, and the epitaxial layer has a thickness of from 0.2 to $1.0\text{ }\mu\text{m}$ and has a surface on which fewer than 30 LLS defects with a size of more than $0.085\text{ }\mu\text{m}$ can be detected.

After the deposition of the epitaxial layer, the semiconductor wafer, preferably in an atmosphere of hydrogen, is brought to a discharge temperature of preferably from 850 to 950°C and discharged from the deposition reactor.

It is possible to coat at least 50, preferably up to 200, substrate wafers in succession before the deposition reactor has to be cleaned with an etching gas or a plasma.

Semiconductor wafers produced according to the invention were compared with conventionally produced semiconductor wafers with regard to LLSs.

15 DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS
Example:

The semiconductor wafers produced according to the invention comprised a substrate wafer made of silicon with a resistivity of 12 Ωcm (p^- -type doping), on which an epitaxial layer having a layer thickness of 0.5 μm and a resistivity of 1.5 Ωcm had been grown. The deposition temperature was from 1130 to 1190°C. The substrate wafers were of type I and type II.

25 In the case of the conventionally produced semiconductor wafers, the substrate wafers originated from a single crystal pulled according to the Czochralski method without any doping with nitrogen. Substrate wafers from a single crystal pulled in this way are referred to below as reference I substrate wafers, if the single crystal had been cooled without forced cooling. In the case of the substrate wafers referred to as reference II substrate wafers, the corresponding single crystal was subjected to forced cooling. The epitaxial layer was deposited under the same conditions as those prevailing for the semiconductor wafers produced according to the invention.

**Semiconductor wafer with a thin epitaxial silicon
layer, and production process**

The invention relates to a semiconductor wafer with a
5 thin epitaxial layer, and a process for producing the
semiconductor wafer by depositing the layer on a
substrate wafer made of silicon.

At the present time intensive investigations are under
10 way with the aim of establishing which features
semiconductor wafers with an epitaxial layer have to have
in order to qualify them as a base material for the
production of modern CMOS components. According to the
publication in Jpn. J. Appl. Phys. Vol. 36 (1997), pp.
15 2565-2570, a semiconductor wafer comprising a p⁻-doped
substrate wafer and a likewise p⁻-doped epitaxial layer
having a thickness of 1 μm is particularly suitable for
large scale integrated CMOS applications. This appraisal
is also supported by the publication in Electrochemical
20 Society Proceedings Volume 98-1, pp. 855-861. However,
this paper also draws attention to light-scattering
defects (light point defects) on the surface which occur
in a semiconductor wafer with a thin epitaxial layer but
do not adversely affect the GOI (gate oxide integrity).
25 The abovementioned defects are called LLSS (localized
light scatterers) by experts. Despite their indifferent
behavior with regard to the GOI, the LLSS are undesirable
to manufacturers of integrated circuits, which is also
demonstrated by the fact that the ITRS (International
30 Roadmap For Semiconductors) demands that the number of
LLSS with a size of greater than or equal to 0.085 μm be
less than or equal to 38 per semiconductor wafer with an
epitaxial layer. This requirement applies to 0.18 μm
technology and it must be assumed that as miniaturization
35 advances (0.13 μm and below), an even more stringent
requirement will be imposed on the number of LLSS.
Moreover, the limit value of 38 LLSS represents a maximum
value and it should be taken into account that the number
required for an industrial process capability must be
40 significantly less than that.

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The object of the invention was to provide a semiconductor wafer with an epitaxial layer which is suitable for modern CMOS applications, has a particularly small number of LLSS and requires comparatively low production costs. The object of the invention is, moreover, to specify a process for producing the semiconductor wafer.

The invention relates to a semiconductor wafer, comprising a substrate wafer made of silicon and an epitaxial layer deposited thereon, which is characterized in that the substrate wafer has a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \cdot 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from $1 \cdot 10^{13}$ to $5 \cdot 10^{15} \text{ atcm}^{-3}$, and the epitaxial layer has a thickness of from 0.2 to 1.0 μm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.

The invention also relates to a process for producing a semiconductor wafer with an epitaxial layer by depositing the layer on a substrate wafer made of silicon, which is characterized by a sequence of steps comprising: the provision of the substrate wafer, the substrate wafer having a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \cdot 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from $1 \cdot 10^{13}$ to $5 \cdot 10^{15} \text{ atcm}^{-3}$; the heating of the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C; and immediately after the deposition temperature has been reached, the deposition of the epitaxial layer with a thickness of from 0.2 to 1.0 μm .

Investigations by the inventors have revealed that the combination of the abovementioned process steps and the fact of the abovementioned material parameters being taken into account afford a semiconductor wafer with an epitaxial layer which wholly satisfies the requirements imposed. With regard to the supposition that can be derived from the abovementioned prior art, according to which the number of LLSS can be kept low only by having

the thickest possible epitaxial layer ($\geq 3 \mu\text{m}$), the result of the investigations is surprising because it shows that extremely low LLSs densities are possible even with layer thicknesses of from 0.2 to 1 μm . The small layer thicknesses and the fact that the proposed process manages without a so-called baking step before the deposition of the epitaxial layer account for a distinct cost advantage over known processes. Thus, the throughput of semiconductor wafers per hour can be increased by up to threefold.

In order to achieve the required properties with regard to the LLSs density, a substrate wafer is required which has a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \cdot 10^{17} \text{ atcm}^{-3}$, particularly preferably of less than $6.5 \cdot 10^{17} \text{ atcm}^{-3}$, and a nitrogen concentration of from $1 \cdot 10^{13}$ to $5 \cdot 10^{15} \text{ atcm}^{-3}$, particularly preferably of from $1 \cdot 10^{14}$ to $5 \cdot 10^{14} \text{ cm}^{-3}$, and is preferably cut from a single crystal that has been pulled according to the Czochralski method. As far as the deposition of the epitaxial layer is concerned, it is important that deposition be effected at a deposition temperature of from 1120 to 1200°C, with account being taken of the type of substrate wafer.

In this case, an elevated deposition temperature has the fundamental advantage of reducing so-called "area counts", that is to say large defects on the epitaxial layer which can lead to losses in yield for semiconductor component manufacturers.

A single crystal from which substrate wafers having the desired properties can be separated can be produced for example according to a process as described in DE-198 23 962 A. In the process, the single crystal is pulled from a melt according to the Czochralski method and, during this, is additionally doped with nitrogen. In accordance with one embodiment of the invention, at least 90 min elapse before single crystal material that has just crystallized has passed through the temperature range from 1050 to 900°C. This is normally the case when the single crystal cools by itself, in other words forced cooling of the single crystal is dispensed with. The

epitaxial layer is deposited on a substrate wafer which originates from a single crystal pulled in such a way and is referred to below as a type I substrate wafer, at a deposition temperature of from 1120 to 1170°C, preferably from 1130 to 1160°C.

In accordance with a further embodiment of the invention, the single crystal is pulled according to the Czochralski process and subjected to forced cooling in this case. As a result, at most 40 min elapse before single crystal material that has just crystallized has passed through the temperature range from 1050 to 900°C. The pulling installation must be provided with a forced cooling arrangement in order to ensure that the single crystal is cooled rapidly. A cooling apparatus in accordance with EP-725 169 A1 is preferably used during the pulling of the single crystal. The epitaxial layer is deposited on a substrate wafer which originates from a single crystal pulled in such a way and is referred to below as a type II substrate wafer, at a deposition temperature of from 1120 to 1200°C, preferably from 1130 to 1190°C, which corresponds to a distinctly wider process window in the epitaxial deposition by comparison with type I and thus distinctly facilitates optimization with regard to economic efficiency.

For the deposition of the epitaxial layer, the substrate wafer is loaded into a deposition reactor. A single-wafer reactor with an automatic wafer loading and discharging mechanism is preferred. The temperature in the reactor should already have a comparatively high value, at the very least 800°C, in the course of loading. A temperature of at least 850°C is preferred, and a temperature of at least 900°C is particularly preferred.

The substrate wafer is subsequently heated to a deposition temperature in a gas atmosphere. The gas atmosphere is preferably selected from a group of gases which includes hydrogen, argon, helium and any desired mixtures of the gases mentioned. A gas atmosphere of hydrogen is particularly preferred.

As soon as the deposition temperature has been reached, the deposition of the epitaxial layer with a thickness of from 0.2 to 1 μm , preferably from 0.3 to 0.6 μm , is begun by an atmosphere of deposition gas and dopant gas being
5 added to the gas atmosphere. A so-called baking step, in which the substrate wafer is kept at deposition temperature in the gas atmosphere for a period of time, for example from 5 to 60 s, is not performed. The deposition gas is preferably selected from a group of
10 gases which includes trichlorosilane, silane, dichlorosilane, tetrachloro-silane and any desired mixtures of the gases mentioned. Trichlorosilane is particularly preferred. The dopant gas is preferably selected from a group of gases which includes diborane,
15 phosphine and arsine. Diborane is particularly preferred.

The deposition time is preferably from 1 to 10 s, particularly preferably from 1 to 5 s. Preference is given, moreover, to setting the resistivity of the
20 epitaxial layer to from 0.5 to 50 Ωcm .

After the deposition of the epitaxial layer, the semiconductor wafer, preferably in an atmosphere of hydrogen, is brought to a discharge temperature of
25 preferably from 850 to 950°C and discharged from the deposition reactor.

It is possible to coat at least 50, preferably up to 200, substrate wafers in succession before the deposition
30 reactor has to be cleaned with an etching gas or a plasma.

Semiconductor wafers produced according to the invention were compared with conventionally produced semiconductor
35 wafers with regard to LLSSs.

Example:

The semiconductor wafers produced according to the
40 invention comprised a substrate wafer made of silicon with a resistivity of 12 Ωcm (p^- -type doping), on which

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an epitaxial layer having a layer thickness of 0.5 μm and a resistivity of 1.5 Ωcm had been grown. The deposition temperature was from 1130 to 1190°C. The substrate wafers were of type I and type II.

5

- In the case of the conventionally produced semiconductor wafers, the substrate wafers originated from a single crystal pulled according to the Czochralski method without any doping with nitrogen. Substrate wafers from a single crystal pulled in this way are referred to below as reference I substrate wafers, if the single crystal had been cooled without forced cooling. In the case of the substrate wafers referred to as reference II substrate wafers, the corresponding single crystal was subjected to forced cooling. The epitaxial layer was deposited under the same conditions as those prevailing for the semiconductor wafers produced according to the invention.
- Tables 1 and 2 below verify that the combined selection of substrate wafer and deposition temperature is of crucial importance when what matters is minimizing the number of LLSs.

Table 1:

LLS>0.085 μm	Type I substrate wafer ^{*)}	Reference I substrate wafer ^{*)}
1130°C deposition temp.	18 (+)	40 (-)
1190°C deposition temp	98 (-)	1167 (-)

Table 2:

LLS>0.085 μm	Type II substrate wafer ^{*)}	Reference II substrate wafer ^{*)}
1130°C deposition temp.	15 (+)	820 (-)
1190°C deposition temp	12 (+)	1389 (-)

^{*)} +/-: satisfies/does not satisfy the requirements of the most modern generations of components.

Furthermore, the dramatic throughput advantage of the wafers produced according to the invention compared with wafers that are epitaxially coated in a conventional manner can be seen from Table 3. The throughput advantage results directly in a corresponding cost advantage.

Table 3:

	Semiconductor wafer according to the invention	Reference wafer ***)
Throughput (wafers/hour)**)	90	30
Relative costs of the epitaxial coating per wafer	0.33	1

***) for a 3-chamber single-wafer reactor

***) 3 μm standard epitaxy

Patent Claims:

1. A semiconductor wafer, comprising a substrate wafer made of silicon and an epitaxial layer deposited thereon, characterized in that the substrate wafer has a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from 1×10^{13} to $5 \times 10^{15} \text{ atcm}^{-3}$, and the epitaxial layer has a thickness of from 0.2 to 1.0 μm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.
2. The semiconductor wafer as claimed in claim 1, characterized in that the oxygen concentration of the substrate wafer is less than $6.5 \times 10^{17} \text{ atcm}^{-3}$.
3. The semiconductor wafer as claimed in claim 1 or claim 2, characterized in that the nitrogen concentration of the substrate wafer lies in a range of from 1×10^{14} to $5 \times 10^{14} \text{ atcm}^{-3}$.
4. A process for producing a semiconductor wafer with an epitaxial layer by depositing the layer on a substrate wafer made of silicon, characterized by a sequence of steps comprising:
the provision of the substrate wafer, the substrate wafer having a resistivity of from 0.1 to 50 Ωcm , an oxygen concentration of less than $7.5 \times 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from 1×10^{13} to $5 \times 10^{15} \text{ atcm}^{-3}$;
the heating of the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C; and
immediately after the deposition temperature has been reached, the deposition of the epitaxial layer with a thickness of from 0.2 to 1.0 μm .
5. The process as claimed in claim 4, characterized in that a single crystal is pulled from a melt in accordance with the Czochralski process, and at least 90 min elapse before the single crystal has passed through the temperature range from 1050 to

900°C, the single crystal serving as a source for the provision of the substrate wafer, and the deposition temperature during the deposition of the epitaxial layer is from 1120 to 1170°C.

6. The process as claimed in claim 5, characterized in that the deposition temperature is from 1130 to 1160°C.

- 10 7. The process as claimed in claim 4, characterized in
that a single crystal is pulled from a melt in
accordance with the Czochralski process and not more
than 40 min elapse before the single crystal, with
application of forced cooling, has passed through
15 the temperature range from 1050 to 900°C, the single
crystal serving as a source for the provision of the
substrate wafer, and the deposition temperature
during the deposition of the epitaxial layer is from
1120 to 1200°C.

8. The process as claimed in claim 7, characterized in that the deposition temperature is from 1130 to 1190°C.

- 25 9. The process as claimed in one of claims 4 to 8,
characterized in that the substrate wafer is heated
to the deposition temperature in a gas atmosphere,
the gas atmosphere being selected from a group of
gases which includes hydrogen, argon, helium and any
30 desired mixtures of the gases mentioned.

10. The process as claimed in one of claims 4 to 9, characterized in that the epitaxial layer is deposited in a deposition atmosphere containing a deposition gas and a dopant gas, the deposition gas being selected from a group of gases which includes trichlorosilane, silane, dichlorosilane, tetrachlorosilane and any desired mixtures of the gases mentioned, and the dopant gas being selected from a group of gases which includes diborane, phosphine and arsine.

- 40 from a group of gases which includes diborane,
phosphine and arsine.

11. The process as claimed in one of claims 4 to 10, characterized in that the epitaxial layer is deposited within a deposition time of from 1 to 10 s.

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12. The process as claimed in one of claims 4 to 11, characterized in that the deposition reactor is subjected to cleaning with an etching gas or plasma at the earliest after an epitaxial layer has been deposited on 50 substrate wafers in succession.

10

Country	Year	Population (millions)	Urban population (millions)	Urban population (%)	Population density (per sq km)	Population density (per sq mile)
Algeria	1980	10.0	4.0	40.0	100	260
Algeria	1985	10.5	4.5	42.9	105	272
Algeria	1990	11.0	5.0	45.5	110	284
Algeria	1995	11.5	5.5	47.8	115	297
Algeria	2000	12.0	6.0	50.0	120	310
Algeria	2005	12.5	6.5	52.0	125	323
Algeria	2010	13.0	7.0	53.8	130	336
Algeria	2015	13.5	7.5	55.6	135	349
Algeria	2020	14.0	8.0	57.1	140	362
Algeria	2025	14.5	8.5	58.6	145	375
Algeria	2030	15.0	9.0	60.0	150	388
Algeria	2035	15.5	9.5	61.3	155	401
Algeria	2040	16.0	10.0	62.5	160	414
Algeria	2045	16.5	10.5	63.6	165	427
Algeria	2050	17.0	11.0	64.7	170	440
Algeria	2055	17.5	11.5	65.7	175	453
Algeria	2060	18.0	12.0	66.7	180	466
Algeria	2065	18.5	12.5	67.6	185	479
Algeria	2070	19.0	13.0	68.4	190	492
Algeria	2075	19.5	13.5	69.2	195	505
Algeria	2080	20.0	14.0	70.0	200	518
Algeria	2085	20.5	14.5	70.7	205	531
Algeria	2090	21.0	15.0	71.4	210	544
Algeria	2095	21.5	15.5	72.1	215	557
Algeria	2100	22.0	16.0	72.7	220	570
Algeria	2105	22.5	16.5	73.3	225	583
Algeria	2110	23.0	17.0	73.9	230	596
Algeria	2115	23.5	17.5	74.5	235	609
Algeria	2120	24.0	18.0	75.0	240	622
Algeria	2125	24.5	18.5	75.5	245	635
Algeria	2130	25.0	19.0	76.0	250	648
Algeria	2135	25.5	19.5	76.5	255	661
Algeria	2140	26.0	20.0	76.9	260	674
Algeria	2145	26.5	20.5	77.3	265	687
Algeria	2150	27.0	21.0	77.8	270	700
Algeria	2155	27.5	21.5	78.2	275	713
Algeria	2160	28.0	22.0	78.6	280	726
Algeria	2165	28.5	22.5	78.9	285	739
Algeria	2170	29.0	23.0	79.3	290	752
Algeria	2175	29.5	23.5	79.7	295	765
Algeria	2180	30.0	24.0	80.0	300	778
Algeria	2185	30.5	24.5	80.3	305	791
Algeria	2190	31.0	25.0	80.6	310	804
Algeria	2195	31.5	25.5	81.0	315	817
Algeria	2200	32.0	26.0	81.3	320	830
Algeria	2205	32.5	26.5	81.6	325	843
Algeria	2210	33.0	27.0	81.8	330	856
Algeria	2215	33.5	27.5	82.1	335	869
Algeria	2220	34.0	28.0	82.4	340	882
Algeria	2225	34.5	28.5	82.6	345	895
Algeria	2230	35.0	29.0	82.9	350	908
Algeria	2235	35.5	29.5	83.1	355	921
Algeria	2240	36.0	30.0	83.3	360	934
Algeria	2245	36.5	30.5	83.6	365	947
Algeria	2250					

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, REINHARD SCHAUER;
DR. MARKUS BLIETZ; DR. WILFRIED VON AMMON; DR. RUDIGER SCHMOLKE,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint
inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought
on the invention entitled:

SEMICONDUCTOR WAFER COMPRISING A THIN EPITAXIAL
SILICON LAYER AND METHOD FOR PRODUCING SAME

the specification of which (check only one item below):

- ☐ is attached hereto.
- ☐ was filed as United States application
Serial No. _____
on _____,
and was amended
on _____ (if applicable).
- ☒ was filed as PCT international application
Number PCT/EP00/01800 filed
on MARCH 2, 2000
and was amended under PCT Article 19
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the
claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in
accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for
patent or inventor's certificate or of any PCT international application(s) designating at least one country other than
the United States of America listed below and have also identified below any foreign application(s) for patent or
inventor's certificate or any PCT international application(s) designating at least one country other than the United
States of America filed by me on the same subject matter having a filing date before that of the application(s) of
which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
GERMANY	199 09 557.4	4 MARCH 1999	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
GERMANY	100 04 623 1	3 FEBRUARY 2000	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NUMBER
SCHAUER ET AL 1 PCT

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application Number)

(Filing Date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS (Check One)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)		

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration numbers):

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201

R. Schauer

SIGNATURE OF INVENTOR 202

M. Hatz

DATE

July 11, 2001

DATE

July 11, 2001

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NUMBER
SCHAUER ET AL 1 PCT

2	FULL NAME OF INVENTOR	FAMILY NAME <u>von AMMON</u>	FIRST GIVEN NAME <u>WILFRIED</u>	SECOND GIVEN NAME
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2	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
0	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
6	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
2	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
0	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
7	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
2	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
0	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
8	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
2	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
0	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
9	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon

SIGNATURE OF INVENTOR 204 <i>Wilfried v. Ammon</i>	SIGNATURE OF INVENTOR 205 <i>Rüdiger Schmölke</i>	SIGNATURE OF INVENTOR 206
DATE <i>July 11, 2001</i>	DATE <i>July 16, 2001</i>	DATE
SIGNATURE OF INVENTOR 207	SIGNATURE OF INVENTOR 208	SIGNATURE OF INVENTOR 209
DATE	DATE	DATE